



# TECHNICAL BRIEF

## BUILT-IN-TEST

### *Design and Optimization Guidelines*

*Published by the Office of the Assistant Secretary of the Navy  
(Research, Development & Acquisition) Acquisition and Business Management*

October 2001  
TB # ABM 1001-01



## Foreword

A primary goal of the ASN (RD&A) Strategic Plan is to acquire, interpret and share technical information and provide expert consultation to continuously improve acquisition practices. To implement this goal, the ASN (RD&A) Acquisition and Business Management Directorate will periodically issue technical briefs.

The intent of this technical brief is to assist our Navy managers, designers and testers with the best possible information regarding built-in-test. This technical brief is a joint effort between senior technical experts within the Navy and industry. The Navy would like to recognize the contributions of the following individuals and organizations to this technical brief: Dennis Hecht, Stanley Ofsthun, Norman Dauderman, The Boeing Company, St. Louis; Howard Perlstein, Chau Mai, Litton Guidance & Control Systems; and the Naval Air Systems Command (AIR 4.1.6).

I solicit your inputs for technical issues that you, the user, would like to see addressed in future technical briefs. You can submit your comments on the ABM homepage at [www.abm.rda.hq.navy.mil](http://www.abm.rda.hq.navy.mil).

R. E. Cowley  
Rear Admiral, SC, U.S. Navy  
Deputy for Acquisition and Business  
Management



# Table of Contents

---

<b>PURPOSE</b> .....	<b>1</b>
<b>DESCRIPTION</b> .....	<b>1</b>
<b>MANAGEMENT</b> .....	<b>1</b>
<b>DESIGN</b> .....	<b>5</b>
<b>TEST</b> .....	<b>10</b>
<b>“WATCH-OUT-FORS”</b> .....	<b>12</b>
<b>APPENDIX A Case Study</b> .....	<b>A-3</b>
<b>APPENDIX B References</b> .....	<b>B-1</b>

## PURPOSE

The purpose of this technical brief is to identify best practices in the areas of management, design and test that will assist in improving the reliability of fielded Built-In-Test (BIT) capabilities. The benefits of BIT include reduced requirements for external test equipment, fewer interfaces between the system and the external world, less damage from invasive inputs, reduced skill level of maintenance personnel required, rapid troubleshooting, reduced downtime, more accurate testing, improved status-monitoring and readiness and reduced life-cycle cost. However, if the BIT is not properly designed, these benefits can be negated by high false alarm rates, which lead to unnecessary maintenance actions.

## DESCRIPTION

BIT equipment provides "built in" monitoring, fault detection and isolation capabilities as integral features of the system design. BIT uses internal system hardware and software to test the system or its subsystems. It often uses internal microprocessors and self-test software to isolate failures.

It can be supplemented with embedded "expert system" technology that incorporates diagnostic logic into the prime system (as available based on platform and program resources) or the external support system. These supplemental capabilities should be used to address specific BIT deficiencies that cannot be effectively addressed via other means; they are not a substitute for good BIT design practices.

## MANAGEMENT

Prior to BIT design, a strategy needs to be established for achievement of BIT goals and objectives. The following provides BIT fundamental management functions and the implementing best practices.

Management Considerations	Best Practices
<p><b>BIT Concepts/ Requirements</b> - BIT concepts can have a major impact on the system design approach. Failure to establish a BIT philosophy early in the program will result in a BIT implementation that evolves in a piecemeal and inefficient manner.</p> <p><i>(continued on next page)</i></p>	<ul style="list-style-type: none"><li>• A BIT Integrated Product Team (IPT) is established, including diagnostic experts from the prime contractor and all major equipment vendors, to coordinate BIT issues throughout the life cycle. The BIT IPT develops a detailed BIT approach prior to design start (e.g., by the Systems Requirements Review).</li><li>• The need for BIT is driven by both operational requirements (e.g., availability, turnaround times) and maintenance requirements (e.g., the maintenance concept, maintenance man-hours per flight hours). Proper balance between these requirements is essential to achieving an effective and affordable implementation.</li><li>• False Alarm (FA) performance is tracked throughout development, qualification, flight testing and field</li></ul>

Management Considerations	Best Practices
	<p>operations, with a well defined growth curve and firm ground rules established.</p> <ul style="list-style-type: none"> <li>• BIT is planned in the system design for all operation and maintenance levels.</li> <li>• Although the specific test capabilities that will be used at the various maintenance levels may be developed throughout the life cycle, test planning occurs concurrently with the design. Detailed attention is paid to test verticality principles, assuring that tests performed using BIT at higher levels of maintenance (e.g., factory or depot levels) will also be used at lower levels of maintenance (i.e., Intermediate and Organizational levels), as applicable. As the design progresses, this attention is expanded to assure that corresponding tests across maintenance levels also adhere to principles calling for wider tolerances at lower levels of maintenance.</li> <li>• An approach is developed to monitor production testing and field maintenance actions to determine fault detection and fault isolation effectiveness.</li> </ul>
<p><b>Trade Studies and Associated Design Analyses</b> - must be completed before a cost-effective BIT design approach can be developed. It is critical for effective BIT design to include test and production disciplines in these studies and analyses to determine optimum approaches. Often, production cost can be prohibitive if the needs of system integration and test functions are not considered.</p> <p><i>(continued on next page)</i></p>	<ul style="list-style-type: none"> <li>• The operational and maintenance requirements of performance monitoring, fault detection and localization are understood and interpreted, with tradeoffs between MTBF, mission reliability, cost, weight, and volume, to determine the type and depth of BIT needed.</li> <li>• System assessments consider the additional hardware and software functions needed to implement BIT.</li> <li>• A thorough testability analysis, including BIT, is performed to guide the system design. This includes a quantitative prediction of Fault Detection/Fault Isolation at each level of maintenance (consistent with the target support concept), a qualitative assessment of false alarm susceptibility (using design checklists), a Failure Modes, Effects and Criticality Analysis (FMECA) and an initial evaluation of test verticality.</li> <li>• Alternative diagnostics concepts are evaluated, including the use of automatic test equipment, manual test techniques, or mixes of these approaches along with BIT. These evaluations include: <ul style="list-style-type: none"> <li>– A determination of the sensitivity of system readiness parameters to variations in key testability parameters including BIT fault detection and isolation as well as false alarm rates.</li> <li>– A determination of life cycle costs sensitivity to variations in key testability parameters.</li> </ul> </li> </ul>

Management Considerations	Best Practices
	<ul style="list-style-type: none"> <li>– An estimate of the manpower and personnel implications of alternative diagnostic concepts in terms of direct maintenance man-hours per operating hour, job classifications, skill levels and experience required at each level of maintenance.</li> <li>– An estimate of technical risk associated with each concept.</li> <li>• A FMECA is performed as a part of the BIT design effort to identify failures that are critical to system performance, and determine which failures should be detected using BIT.</li> <li>• A Worst Case Circuit Tolerance Analysis is performed on the system and used in the BIT design effort to identify tolerance requirements that ensure design stability during worst case Design Reference Mission Profile conditions.</li> <li>• BIT design for systems that are dormant or unpowered for a major portion of their deployment period considers the effects on system availability from dormant system failures and the probability of system failures occurring during the cumulative power-on time required to perform BIT tests.</li> </ul>
<p><b>Design Reviews</b> – are conducted to assess BIT design progress against requirements for specific time intervals during the development phase.</p> <p><i>(continued on next page)</i></p>	<ul style="list-style-type: none"> <li>• Preliminary and Critical Design Reviews (PDR/CDR) should be conducted at both prime and subcontractors, and are held in conjunction with reliability, maintainability and logistic support reviews. These design reviews should consider the following: <ul style="list-style-type: none"> <li>– BIT philosophy, fault isolation and partitioning methods, and threshold adjustment methods.</li> <li>– Conformance of the design to the BIT approach by senior designers as well as logistics, test, production and field personnel.</li> <li>– Structured verification of BIT as a part of the initial systems integration and early measurement in the use environment by end item users. This includes tracking false alarms throughout development and implementing engineering investigations/corrective action processes in the same manner as hardware failures.</li> <li>– Estimated impact of the diagnostic concept on readiness, life cycle costs, manpower and training.</li> <li>– Assessment of performance monitoring, BIT and off-line test performance requirements and constraints to ensure completeness and consistency.</li> <li>– Identify which testability design guides, analysis procedures or automated tools are used.</li> <li>– The extent to which testability criteria are being met and</li> </ul> </li> </ul>

Management Considerations	Best Practices
	<p>the identification of any technical limitations or cost considerations inhibiting full implementation.</p> <ul style="list-style-type: none"> <li>– Adequacy of FMECA.</li> <li>– Integration of the BIT hardware and BIT software development and test efforts.</li> <li>– Review effectiveness of the BIT interface and tailored data provided to operator and maintenance personnel.</li> <li>– BIT fault detection and fault isolation measures are used for automatic test generation and test grading.</li> <li>– BIT fault detection and isolation performance criteria to determine compliance to BIT requirements.</li> <li>– Include BIT parameters in testability and/or maintainability demonstrations plans and procedures.</li> <li>– Plans for evaluating the impact of subsequent design changes on BIT (e.g., Engineering Change Proposals or Class II changes that require assurance that form, fit, function and interface are unaffected).</li> <li>– Production design studies to define the use of BIT in manufacturing inspection, test, and evaluation.</li> <li>– BIT self test capability.</li> </ul>
<p><b>Fault Tolerant Designs</b> – are increasingly dependent on the ability to detect, isolate, and recover from malfunctions as they occur.</p>	<ul style="list-style-type: none"> <li>• BIT features and the overall testability of the design are tradeoffs that are part of the fault tolerant design process.</li> <li>• To properly design a fault tolerant system, including a diagnostic scheme, requires that a FMECA be performed.</li> <li>• The BIT in a fault tolerant system design must: <ul style="list-style-type: none"> <li>– Maintain a real-time status of the system’s assets (both on-line and off-line equipment).</li> <li>– Provide the operator with the status of available system assets.</li> <li>– Maintain a record of hardware faults and reconfiguration events required for system recovery during the mission for post-mission evaluation and corrective maintenance.</li> </ul> </li> <li>• Failures that can affect BIT performance, such as drift, should be clearly defined in the fault detection and isolation analysis.</li> <li>• A formal process should be in place to ensure that test verticality is maintained from one maintenance level to the next.</li> </ul>
<p><b>Expert Systems</b> - consist of rule based artificial intelligence architecture. With</p>	<ul style="list-style-type: none"> <li>• Based on actual experience during test programs, rules are added to the system to make decisions regarding which BIT codes will be set on the maintenance control panel to drive</li> </ul>

Management Considerations	Best Practices
<p>information available to the expert system, it filters BIT indications through its rule-based logic and detailed data on weapon system operating status. For example, BIT may indicate that four unrelated WRA's have failed. The expert system knows that the probability of these four WRA's failing simultaneously is remote. It also knows that these four WRA's are powered by the same power supply. Therefore, instead of setting four BIT codes to replace each of the four WRA's, it sets one BIT code to replace the common power supply. In this case, the expert system correctly identified the bad WRA and prevented four no-defect-found removals.</p>	<p>maintenance actions.</p> <ul style="list-style-type: none"> <li>• The expert system provides detailed information so that it: <ul style="list-style-type: none"> <li>– Knows exactly what the weapon system is doing (e.g., aircraft attitude, altitude, airspeed, engine settings, temperature, vibration, G forces). This information is made available to individual equipment for possible inclusion in their non-volatile fault logs to assist diagnostics at the various maintenance levels.</li> <li>– Knows how equipments and subsystems are wired together including their operating parameters.</li> </ul> </li> </ul>

## DESIGN

The following provides key design parameters and the associated best practices. The early implementation of BIT design is essential. The BIT concept must be established as part of the maintenance concept, which is normally defined no later than the weapon system Preliminary Design Review. This enables detail design for testability and BIT to proceed toward Critical Design Review. At Critical Design Review, the design becomes firm, reflecting the final partitioning of the system performance functions into the various hardware levels (e.g., Organizational, Intermediate and Depot level units). At this point in the development cycle, any design change, such as to the partitioning to enhance testability is severely compromised due to cost increases and schedule delays. The following tables provide descriptions and best practices for key BIT design functions.

Design Considerations	Best Practices
<p>BIT Software</p> <p><i>(continued on next page)</i></p>	<ul style="list-style-type: none"> <li>• BIT software is partitioned from other software to allow separate updates, enhancing release cycles. Develop BIT software: <ul style="list-style-type: none"> <li>– For most flexible options (voting logic, sampling variations, filtering, etc.), to verify proper operation and</li> </ul> </li> </ul>

Design Considerations	
	<p>identification of a failure or its cause.</p> <ul style="list-style-type: none"> <li>- To minimize BIT hardware.</li> <li>- To record BIT parameters.</li> <li>- To achieve BIT performance accountability and continuous improvement by requiring the BIT software to be unbundled from the operational flight program software. As BIT anomalies occur, BIT updates can be implemented without waiting for the next operational flight program release cycle. Both aircraft and equipment BIT software should segregate test parameters and/or code into a separately controlled software configuration item.</li> <li>- Allow wrap arounds, comparisons and computations.</li> </ul>
Multiplexing	<ul style="list-style-type: none"> <li>• Use multiplexing to simplify BIT circuitry. Digital processing allows performance of BIT tests in the same paths as ones used for primary functions, through multiplexing techniques, requiring little added hardware.</li> </ul>
Processors	<ul style="list-style-type: none"> <li>• Use processors to provide powerful and versatile real time or high speed verification of proper operation and the intelligence to analyze multiple failure indications to pinpoint the primary cause of failure. They enable mutual “watchdog” checking of the other modules for best detection and isolation. Their use involves little additional hardware, except for memory required to store the BIT software.</li> </ul>
Fault Ambiguity Group	<ul style="list-style-type: none"> <li>• Size the fault ambiguity group considering: <ul style="list-style-type: none"> <li>- Mission requirements for reliability, repair time, down time, false alarm rate, etc.</li> <li>- Requirements for test equipment/manning at intermediate and depot maintenance levels.</li> </ul> </li> </ul>
BIT Detection	<ul style="list-style-type: none"> <li>• BIT goals should provide: <ul style="list-style-type: none"> <li>- 98% detection of all failures.</li> <li>- Isolation to the lowest replaceable unit.</li> <li>- Less than 0.1% false alarms.</li> </ul> </li> </ul>
Weapon Replaceable Assembly Identification	<ul style="list-style-type: none"> <li>• Weapon replaceable assemblies should have a method for indicating whether or not a weapon replaceable assembly is</li> </ul>

Design Considerations	
	installed (e.g., jumper).
High Packaging Density Components	<ul style="list-style-type: none"> <li>• Select high packaging density components (e.g., Application Specific Integrated Circuits (ASICS)) that incorporate some form of BIT into their designs. The assembly (e.g., board, module etc.) that uses such devices integrates these component BIT capabilities with the BIT design.</li> <li>• Adequate BIT must be required for high packaging density components to ensure unambiguous fault detection and isolation. General BIT requirements for all high packaging density component designs provide: <ul style="list-style-type: none"> <li>– The capability to fault isolate the high packaging density components on board 90% of the time.</li> <li>– Functions that allow fault isolation to the board from system level BIT.</li> <li>– A minimum of 4-usable I/O pins reserved for testability purposes.</li> <li>– A minimum of 15% usable gates reserved for testability/BIT circuitry implementation.</li> </ul> </li> <li>• Use Scan techniques (e.g., Scan Path, Scan/Set Logic, Random-Access Scan, etc.) to enhance testability. These techniques incorporate a test circuitry internally to the chip that permits access to many internal nodes through a very few I/O pins, test data can then be entered and read out in a serial fashion mode.</li> </ul>
BIT Thresholds/Constants	<ul style="list-style-type: none"> <li>• Trade-offs are performed to determine the Design Reference Mission Profile based "minimally acceptable operational thresholds" for BIT, which, are typically not the same as the factory acceptance test procedure thresholds used for equipment acceptance in the factory. This allows some flexibility for varying missions and environmental conditions in actual fleet use before a BIT failure indication is set.</li> <li>• BIT thresholds can be independently changed without affecting the system tactical software.</li> <li>• Verify adequacy of the BIT circuit thresholds during development testing.</li> </ul>
"M out of N" Test	<ul style="list-style-type: none"> <li>• The use of an adequate "M out of N" when checking a parameter to allow any momentary or intermittent anomaly to come and go before a BIT failure indication is set (e.g., a ten second interval, not a 10 millisecond interval). This prevents intermittent problems such as those caused by EMI</li> </ul>

Design Considerations	
	and/or dirty power from causing false alarms.
Shutdown Procedures	<ul style="list-style-type: none"> <li>Assure that different shutdown procedures and/or other switching sequences don't set a BIT flag (e.g., shutting down the engine and getting a NO GO for the hydraulic system). These undesirable BIT flags should be addressed via operating software.</li> </ul>
Clock Control	<ul style="list-style-type: none"> <li>When designing a repairable assembly with a free running clock, it is mandatory to have provisions in the design to inhibit the clock and allow clock control to be provided by an external source.</li> </ul>
Shop Repairable Assembly Initialization	<ul style="list-style-type: none"> <li>Any Shop Repairable Assembly (SRA) that contains sequential devices should have the capability of being initialized by external sources via the repairable assembly I/O connector. If this is not possible all the time, then the repairable assembly should have the capability of being initialized via its logic.</li> <li>Use initializeable counters.</li> </ul>
Transparent Latched	<ul style="list-style-type: none"> <li>Use Transparent Latched instead of Flip-Flops where possible. Transparent Latched make logic more testable since they act as buffers, restoring logic levels.</li> </ul>
Long Counter Chains	<ul style="list-style-type: none"> <li>If the design requires a long counter chain (e.g., more than 12 stages), provisions should be made to break up the counter chain so that it can be tested in smaller groups to enhance isolation to a single module.</li> </ul>
Utilization of Test Points	<ul style="list-style-type: none"> <li>Review the SRA design for test point placement, performance verification and diagnostic fault isolation.</li> <li>All test points identified are available through the SRA input/output connector or a test connector.</li> <li>The SRA design provides test points for large fan-in or fan-out circuits and/or networks which have high ambiguity groups.</li> <li>Designs should be limited to fan-outs of</li> </ul>

Design Considerations	
	<p>one less than the device maximum, so external equipment connection should be possible without adversely loading the circuit design.</p> <ul style="list-style-type: none"> <li>• Use test pin(s) to drive all outputs and I/O's to high impedance states. By driving all outputs and I/O's to high impedance states, the output leakage and breakdown parameters can be measured in single step, thus simplifying incoming inspection.</li> </ul>
Wired ANDs and ORs.	<ul style="list-style-type: none"> <li>• The design is reviewed to minimize the number and size of ambiguity groups associated with wired ANDs and/or wired ORs. They are commonly employed to save components, power and achieve better reliability. However, this network configuration is a tradeoff in the size of ambiguity groups that results when failure occurs in the wired network</li> </ul>
ROM/RAM Designs	<ul style="list-style-type: none"> <li>• Chip select signals are brought out as test points so that they can be uniquely tested and verified. Once the chip select signals are verified as operational, the ROMs and RAMs can be uniquely tested and isolated.</li> </ul>
Shop Repairable Assembly Input/Output Design	<ul style="list-style-type: none"> <li>• Permit "safe" shorting of input and output lines. These lines may be grounded either accidentally while testing or on purpose when injecting a failure during test program development. The grounding should not cause permanent circuit damage.</li> </ul>
Power Supply Voltage Sequences	<ul style="list-style-type: none"> <li>• The system is designed to prevent equipment damage due to power supply sequencing.</li> </ul>
Domino Failure Designs	<ul style="list-style-type: none"> <li>• Review the SRA designs to determine if a failure would cause a domino or cascade of failures.</li> </ul>
Feedback and Redundant Loops.	<ul style="list-style-type: none"> <li>• All redundant paths are ideally completely separable and capable of being tested individually.</li> <li>• Systems using analog feedback networks must ensure overall stability when the system is operated open loop.</li> </ul>

Design Considerations	
Number of Logic Families	<ul style="list-style-type: none"> <li>• One logic family is used, where possible. If multiple logic families must be used, then the number per shop reparable assemblies should be kept to a minimum.</li> </ul>
Microprocessor Designs	<ul style="list-style-type: none"> <li>• Provide external control of the following: <ul style="list-style-type: none"> <li>- Clock Line.</li> <li>- Hold Line.</li> <li>- Interrupt Line.</li> </ul> </li> <li>• Provide external access to the following in order to read or inject data: <ul style="list-style-type: none"> <li>- Data Bus.</li> <li>- Address Bus.</li> </ul> </li> </ul>
Mechanical Design	<ul style="list-style-type: none"> <li>• Use the same type connectors on all the printed circuit cards.</li> <li>• Use a keying system that can be defeated for testing purposes.</li> <li>• Use consistent orientation of parts.</li> <li>• Leave space between parts so that removal/replacement can be accomplished without damaging adjacent components.</li> <li>• Standardize the location of power and ground on printed circuit cards.</li> <li>• Test points are brought out to the primary I/O interface. If not feasible, they are brought out to a separate connector. They are not dispersed around the board as pads, posts, wire loops, etc., since they are then difficult to connect to the automated test equipment.</li> </ul>
Test Point Compatibility	<ul style="list-style-type: none"> <li>• Test points are compatible with the test equipment interface characteristics available on existing support equipment (e.g., CASS).</li> </ul>

## TEST

BIT requirements are difficult to verify, even with a formal demonstration test. This is due in part because failure mechanisms that cause transient or intermittent behavior are not easily simulated in a factory/laboratory environment. The laboratory tests, by themselves, typically

provide limited confidence in demonstrating the diagnostic capabilities of a system design. The following test considerations and associated best practices will augment laboratory tests resulting in the maturation of the BIT design and verification of requirements.

Test Considerations	Best Practices
<p><b>BIT Maturation</b> - requires a period of time for identification of problems and corrective action to reach specified performance levels. This “maturing” process is especially true in operational adjustments and validation of test tolerances.</p> <p><i>(continued on next page)</i></p>	<ul style="list-style-type: none"> <li>• A well-planned verification program includes naturally occurring failures during development and subsequent testing.</li> <li>• Allocate adequate test time to establish test tolerances that result in optimum balance between failure detection and false alarms.</li> <li>• Initial BIT Assessment (IBA) in the factory includes a phased approach providing an early indication of the actual hardware and software BIT capability and identifies any BIT problems requiring corrective action. <ul style="list-style-type: none"> <li>– This phased approach includes; (1) performing non-destructive BIT tests at the lowest replaceable unit and higher level assemblies (e.g., WRA/SRU) interfaces/connections, (2) assessing naturally occurring system test failures and the associated BIT indications for corrective actions, and (3) insertion of faults into the system as required to obtain confidence in meeting BIT requirements/goals.</li> <li>– The tests used for these purposes are normally in conjunction with other planned tests such as Reliability Growth Tests and Maintainability/Testability Tests.</li> <li>– Changes resulting from the IBA assessment are implemented in the hardware, software and procedures prior to TECHEVAL.</li> </ul> </li> </ul>
<p><b>Data Tracking, Analysis and Corrective Action System</b> - is an essential part of the BIT maturation process.</p>	<ul style="list-style-type: none"> <li>• A closed-loop data tracking system is implemented to track initial failure occurrences, organizational-level corrective actions, higher-level maintenance actions, and subsequent utilization and performance of repaired and returned items. <ul style="list-style-type: none"> <li>– Data collection is integrated with similar data collection requirements such as for tracking and maintainability.</li> </ul> </li> <li>• Corrective actions are submitted for review and implementation as part of the established engineering change process.</li> </ul>

## “WATCH-OUT-FORS”

The following provides selected lessons learned expressed as “Watch-Out-Fors” that can become traps if not considered in the management design and test of BIT.

- Introducing testability requirements late in the acquisition cycle. This limits fault isolation, fault detection, and BIT capability, in addition to increasing life cycle cost.
- Citing BIT as a 'desired' rather than a 'required' feature in the system specification.
- Unrealistically high BIT effectiveness requirements resulting in unacceptably high false alarm rates.
- BIT design and analyses that fail to consider the effects of Design Reference Mission Profile and worst-case variations of parameters, such as noise, part tolerance, and timing, especially as affected by age.
- Failures in BIT circuits that affect performance of the system.
- Use of unproven state-of-the-art BIT designs.
- No provisions to independently isolate redundant circuits.
- Digital circuits not partitioned from analog circuits.
- Inadequate BIT memory allocation.
- Limitations to BIT coverage/effectiveness caused by:
  - Non-detectable parts (mechanical parts, redundant connector pins, decoupling capacitors, one-shot devices, etc.).
  - Power filtering circuits.
  - Use of special test equipment (e.g., signal generators) to simulate operational input circuit conditions.
  - Interface and/or compatibility problems between some equipment designs (e.g., digital vs analog).
  - Testing constraints that cause failures of one-shot devices, safety related circuits and physically restrained mechanical systems.
  - Methodology used to calculate BIT effectiveness.
- Providing operators periodic or background BIT diagnostic information not needed to conduct their mission. This increases their workload during combat.
- Designing BIT to report a "NO/GO" status during warm-up periods. Instead, have BIT report the system is in warm-up and "Not Ready."
- Leaving engineering level diagnostics software in the system for operational use. These are usually additional BIT fail flags and signal level data that are intended to be incorporated into the software to help develop the BIT capability. If these additional BIT flags are inadvertently left in the equipment, and are activated, the maintenance personnel must work them off to clear the maintenance monitor panel, even though they are reporting items that do not prevent proper system operation.

# **APPENDIX A**

## **Case Study**

## **F/A-18E/F EMD Flight Test BIT Maturation Process**

Although all aspects of BIT design and development are important, the following case study is limited to the Engineering and Manufacturing Development (EMD) test BIT maturation process. In order to ensure that the F/A-18E/F's BIT performance was improved over legacy aircraft, the BIT development and verification processes required changes from those processes previously used. An updated BIT maturation process resulted in a BIT system that is far superior to any other aircraft BIT currently in the fleet.

During flight-testing, BIT had the same priority as other operational performance requirements. Throughout the flight-test period the BIT maturation process:

- Ensures root cause and corrective actions for all deficiencies are determined and implemented in a timely manner.
- Provides top-level management visibility of BIT performance.

### **Management**

Prior to the start of flight-testing, a dedicated BIT team comprised of Navy reliability and maintainability personnel and Boeing Missions Systems personnel was implemented. The BIT team researched and correlated BIT requirements to actual fleet needs. Based on fleet needs and operational scenarios, the BIT team developed a BIT Development/Evaluation Plan. This plan:

- Established the objectives of the BIT program.
- Identified the data collection, analysis, scoring, and reporting processes.
- Identified the anomaly reporting processes.
- Detailed the ground rules for data analysis and reporting.

The BIT team received strong Navy and Boeing management support, and all F/A-18E/F Integrated Product Teams (IPTs) understood the importance of BIT to their functional/operational parameters. This was a paradigm shift for many IPTs. Whenever a system was not meeting its individual requirement, Navy/Boeing Management required the team to track and report their progress towards meeting the required BIT performance.

Throughout the EMD flight test program, the BIT team updated the ground rules, when necessary, and provided the BIT status to both Navy and Boeing F/A-18E/F management. Management ensured that an emphasis was placed on characterizing and correcting all known BIT false alarms at the earliest opportunity. Status reports included:

- An assessment of current BIT status versus requirements.
- The predicted growth based on the projected (known and forthcoming) corrective actions.
- A summary of each integrated product team's performance.
- High false alarm drivers.
- Status of deficiency reports, including:
  - Total.
  - Number open.
  - Number closed.
  - Number with known corrective actions.

## **Data Collection**

Data collection and evaluation was the backbone of the entire BIT maturation process. Boeing and the Navy assigned approximately 20 maintenance knowledgeable supportability personnel to monitor and document the maintenance on all seven EMD airplanes on a two-shift basis. Their task was to observe maintenance as it was performed, to document maintenance relevant data elements, and to verify the accuracy of the contractors' maintenance documentation. After each maintenance action, the monitors completed a Maintenance Monitor Form, which was used to aid in the evaluation of items related to reliability, maintainability, supportability, and BIT. After each flight, the monitors assigned a preliminary Fault Isolate and Detect (FID) code to each aircraft BIT indication and maintenance action. The FID code assigns relevancy for fault detection, fault isolation, and false alarms. All information was maintained in the Aircraft Fault Reporting System database at Boeing. Based on the data collected, the BIT team:

- Coordinated the collection of BIT data by the maintenance monitors.
- Researched every BIT code that was set and correlated them to maintenance actions conducted.
- Coordinated anomalous situations (e.g., a BIT code that did not relate to a maintenance action or that appeared to be false) with IPTs.
- Reviewed detailed BIT data to determine if a deficiency occurred.
- Supported the IPT in preparing the anomaly report and collecting any additional data needed for the BIT anomaly investigation.
- Oversaw all BIT problem area investigations, testing, and subsequent development and implementation of corrective actions.
- Conducted weekly BIT Review Board meetings. During these weekly meetings, the BIT team, along with the IPT engineers and maintenance monitors:
  - Reviewed and updated the FID codes.
  - Reviewed open anomaly reports.
  - Determined the need for new anomaly reports.
  - Re-classified any corrected anomalies.
- Updated the BIT database and used this data to calculate and report BIT performance.
- Maintained a consolidated list of known BIT deficiencies, proposed corrective actions and corrective action implementation dates. Whenever new software loads were introduced, the list was updated. Test engineers and maintenance technicians became very dependent on this list for determining the need to conduct maintenance.

Having one group, the BIT team, focused solely on improving BIT, resulted in significant improvements in the F/A-18E/F BIT over legacy aircraft. This BIT functional area concept allowed for a single group to prioritize BIT false alarms and keep the IPTs focused on resolving BIT issues. Past experience shows that if there is no one group dedicated to the eradication of BIT false alarms, the correction of the false alarms will be given a low priority resulting in an aircraft with a very high BIT false alarm rate.

## **Risk Reduction**

Based on BIT requirements, the BIT team's objectives, and the fleet's needs, risk areas were

identified and presented to Navy and Boeing F/A-18E/F Management. The BIT risks were tracked as a key performance parameter in the F/A-18E/F Air Vehicle Risk Management process. The following are two examples of risks identified and risk mitigation efforts implemented.

Area of Risk	Description	Mitigation
<p>High False Alarm Rate of F/A-18C/D Legacy Avionics Systems.</p>	<p>The F/A-18E/F has many avionics systems common with the F/A-18C/D and other platforms. Poor BIT false alarm performance of these common avionics systems would result in the overall F/A-18E/F avionics system not meeting Operational Requirements Document (ORD) false alarm percentage requirements, even if the F/A-18E/F unique systems performed perfectly during Operational Testing.</p>	<p>Since very few corrective actions could be implemented in the common equipment a different approach had to be developed. To mitigate this risk Boeing developed and implemented a technique for filtering out false alarms while still retaining good detection capability. A database file, known as the Diagnostic File Filter (DFF), was developed to filter known false BIT indications, based on the conditions that cause them to be set. The capability also existed to completely “turn off” a fault code or to selectively inhibit any unique periodic test within a subsystem from setting a fault code. The DFF is loaded in the Memory Unit and subsequently uploaded to the Mission Computers at power-up.</p> <p>The DFF also proved useful in testing the effectiveness of F/A-18E/F avionics BIT fixes prior to final Software Configuration Set (SCS) implementation. The process of enabling and updating BIT rule base filters independently from the airplane SCS permitted expeditious implementation of fixes and the corresponding reduction in false alarm impacts. There were twelve releases of the DFF during EMD. The final release contained BIT filtering for fifty MSP codes, twenty-three of which were common to the F/A-18C/D. The twenty-three common DFF rules have been implemented into the F/A-18C/D.</p>
<p>Inaccurately reporting BIT performance during Operational Testing.</p>	<p>Inexperience with new BIT functionality and the lack of common reporting ground rules may result in an inaccurate assessment of BIT</p>	<p>To mitigate this risk numerous working group sessions were conducted between the Development Testing (DT) BIT team, Commander Operational Test and Evaluation Force representatives, and the</p>

Area of Risk		
	performance during operational testing.	Operational Test (OT) squadron, VX-9. During these meetings, the DT BIT team and the OT BIT analysts developed common ground rules and evaluation processes. This effort provided the OT BIT analysts with pre-evaluation experience of BIT functionality, enabled the OT analysts to use the applicable DT procedures and processes, and opened lines of communication between the DT and OT BIT test personnel.

### BIT False Alarm Performance Results

Improvements in false alarm performance were very slow for the first year of EMD for a number of reasons:

- The primary factor was the schedule dependent phase-in of false alarm fixes based on the next release of software, resulting in implementation delays and slower growth rates. Usually the parent system Operational Flight Program change was developed and implemented by the supplier of the system, whereas, mission computer SCS changes were the responsibility of Boeing. This phased BIT implementation approach is not the desired method for developing BIT software and is not recommended for new development programs. BIT software should be developed concurrent with the operational software, so that they are matured together throughout the BIT hardware/software integration process.
- EMD equipment configurations affected overall airplane BIT growth. Installation and operation of mission systems related equipment was phased in during the EMD flight test program. Newly identified integration anomalies resulted in more false alarms to fix. Each delivered airplane had slightly different configurations, and each presented unique integration issues that had to be dealt with.
- The percentage of BIT functionality that was turned on during the initial phase of EMD also affected the growth rate. The approach used by some of the more complex subsystems was to activate only a portion of the BIT tests during the beginning of flight-testing. As work continued to eliminate problems found with these initial BIT tests, more tests were activated and corrected until all BIT tests were turned on, evaluated, and corrected. As a result, the sequential activation of more BIT tests affected the overall growth rate. At times, growth was negative because problems found with newly activated tests or newly installed systems often offset improvements.

The EMD history of problems identified (225) and solutions incorporated (222) to resolve over 5300 false alarms. The resulting false alarm rate for the F/A-18E/F is approximately one third that of the F/A-18C/D. Since BIT maturation does not end when development testing ends, the BIT maturation effort should continue on into fleet operations by:

- Identifying and correcting deficiencies caused by the fleet environment.
- Verifying corrective actions for previously discovered BIT problems.
- Evaluating BIT performance of software and hardware upgrades.

# **APPENDIX B**

## **References**

## References

MIL-HDBK-388, "*Electronic Reliability Design Handbook*," 1 October 1998.

MIL-HDBK-470A, "*Designing And Developing Maintainable Products And Systems*," 4 August 1997.

MIL-HDBK-2084, "*Department of Defense Handbook for Maintainability of Avionic and Electronic Systems and Equipment*," 31 July 1995.

MIL-HDBK-2165, "*Testability Program for Electronic Systems and Equipment*," 31 July 1995.

NAVAIR Reliability and Maintainability Course Manual, December 1996.

National Defense Industrial Association, Systems Engineering Committee, 3<sup>rd</sup> Annual systems Engineering & Supportability Conference, October 23-26, 2000: "*F/A-18E/F Built-In-Test (BIT) Maturation Process*," Authors: Karen T. Bain and David G. Orwig.